**Objective:**

1. To implement and test a 2-to-4-lines decoder with active-LOW outputs and active-LOW enable input using random gates.
2. To implement and test combinational logic functions using IC 74138 (3-to-8-lines decoder with active-LOW outputs).

**Answer to the Post Lab Question:**

**01.**

Comparison between Experimental results and Prelab results:

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | **Experimental results** | | | | **Prelab results** | | | |
|  |  |  |  |  |  |  |  |  |
| **0 0 0** | **1** | **1** | **1** | **0** | **1** | **1** | **1** | **0** |
| **0 0 1** | **1** | **1** | **0** | **1** | **1** | **1** | **0** | **1** |
| **0 1 0** | **1** | **0** | **1** | **1** | **1** | **0** | **1** | **1** |
| **0 1 1** | **0** | **1** | **1** | **1** | **0** | **1** | **1** | **1** |
| **1 0 0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **1 0 1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **1 1 0** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |
| **1 1 1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

These truth tables are same. So results are verified.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **Experimental Value** | | **Theoretical Value** | |
|  |  |  |  |  |
| **0 0 1 0 0 0** | **0** | **1** | **0** | **1** |
| **0 0 1 0 0 1** | **1** | **0** | **1** | **0** |
| **0 0 1 0 1 0** | **1** | **0** | **1** | **0** |
| **0 0 1 0 1 1** | **0** | **0** | **0** | **0** |
| **0 0 1 1 0 0** | **1** | **0** | **1** | **0** |
| **0 0 1 1 0 1** | **0** | **1** | **0** | **1** |
| **0 0 1 1 1 0** | **0** | **1** | **0** | **1** |
| **0 0 1 1 1 1** | **1** | **1** | **1** | **1** |

These truth tables are same. So results are verified.

**02.**

Structural Verilog code:

**module expt2(input E, A1, A0,**

**output O0, O1, O2, O3);**

**wire w1, w2, w3, w4;**

**nand g1(O0, ~E, ~A1, ~A0),**

**g2(O1, ~E, ~A1, A0),**

**g3(O2, ~E, A1, ~A0),**

**g4(O3, ~E, A1, A0);**

**endmodule**

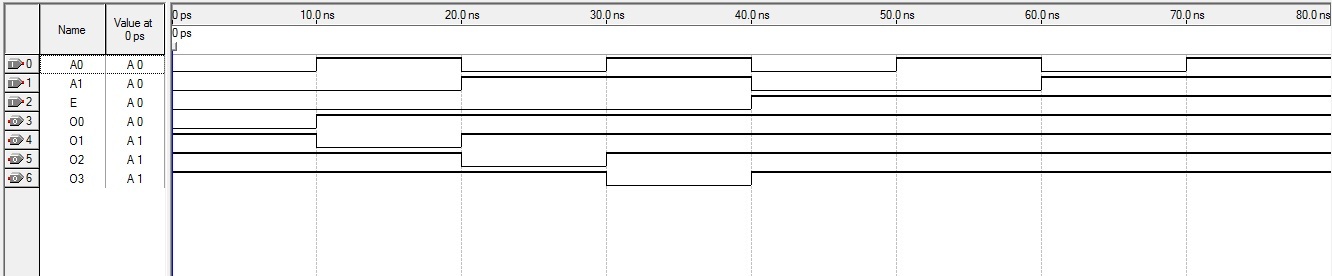


Figure 1: Simulation Waveform

03.

Behavioral Verilog code:

**module expt3(input A0, A1, A2,**

**output S, O0, O1, O2, O3, O4, O5, O6, O7);**

**assign O0 = ~(~A2 & ~A1 & ~A0);**

**assign O1 = ~(~A2 & ~A1 & A0);**

**assign O2 = ~(~A2 & A1 & ~A0);**

**assign O3 = ~(~A2 & A1 & A0);**

**assign O4 = ~(A2 & ~A1 & ~A0);**

**assign O5 = ~(A2 & ~A1 & A0);**

**assign O6 = ~(A2 & A1 & ~A0);**

**assign O7 = ~(A2 & A1 & A0);**

**assign S = O0|O1|O2|O3|O4|O5|O6|O7;**

**endmodule**

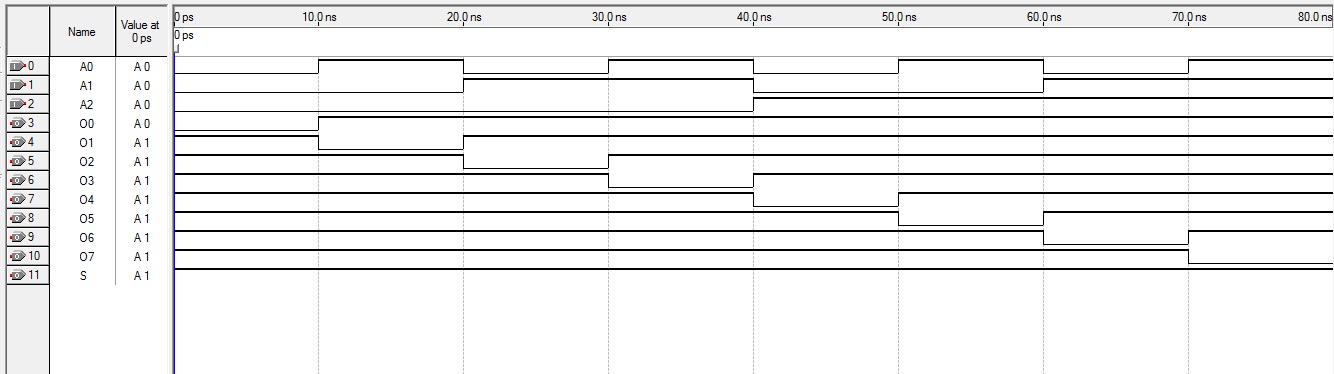
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Figure 2: Simulation Waveform

**Conclusion:**

In this experiment, we have learned how to implement decoder using random gates. We alse implement and test combinational logic functions using IC 74138(3-to-8 lines decoder with active-LOW outputs). We write structural and behavioral Verilog code of these decoders and used Quartus II software to perform simulation.

**EAST WEST UNIVERSITY**

**Semester:** Fall 2017

**Course Number:** CSE 345

**Course Title:** Digital Logic Design

**Experiment No:** 05

**Experiment Title:** Decoder and its use in combinational logic implementation

**Name:** Md. Sakibur Rahman

**ID:** 2014-1-60-032

**Group Number:** 01

**Group IDs:**

2014-1-60-032

2015-1-60-065

2015-1-60-071

2015-1-60-081

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